

This listing of claims replaces all prior versions, and listings, of claims in this application.

Listing of Claims:

1-7. (Cancel)

8. (Currently Amended) A chip resistor comprising:

an insulating substrate having an upper surface and a side surface;

a first conductor pattern formed on the upper surface; and

a resistor element connected to the first conductor pattern; and

a protective coating covering the resistor element;

the first conductor pattern including a thinner-walled portion contacting the upper surface, and a thicker-walled portion connected to the thinner-walled portion and contacting the upper surface, the thinner-walled portion being spaced from the resistor element and extending up to the side surface, the thicker-walled portion contacting the resistor element and being spaced from the side surface;

the thinner-walled portion being positioned entirely outside the protective coating;

the thicker-walled portion being positioned partially outside the protective coating and partially inside the protective coating.

9-10. (Cancel)

11. (New) A chip resistor comprising:

an insulating substrate having an upper surface and a side surface;

a first conductor pattern formed on the upper surface;

a resistor element connected to the first conductor pattern; and

a second conductor pattern extending on the first conductor pattern;

the first conductor pattern including a thinner-walled portion contacting the upper surface, and a thicker-walled portion connected to the thinner-walled portion and contacting the upper surface, the thinner-walled portion being spaced from the resistor element and extending up to the side surface, the thicker-walled portion contacting the resistor element and being spaced from the side surface;

the second conductor pattern contacting both of the thinner-walled portion and the thicker-walled portion.

12. (New) A chip resistor comprising:

an insulating substrate having an upper surface and a side surface;

a first conductor pattern formed on the upper surface; and

a resistor element connected to the first conductor pattern;

the first conductor pattern including a thinner-walled portion contacting the upper surface, and a thicker-walled portion connected to the thinner-walled portion and contacting the upper surface, the thinner-walled portion being spaced from the resistor element and extending

up to the side surface, the thicker-walled portion contacting the resistor element and being spaced from the side surface;

wherein the thinner-walled portion has a thickness of 0.1-3.0 μ m, whereas the thicker-walled portion has a thickness of 5-25 μ m.